Stellaris® LM3S6965 Evaluation Board

User's Manual

EK-LM3S6965-06

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Table of Contents

List of Figures

List of Tables

C H A P T E R 1

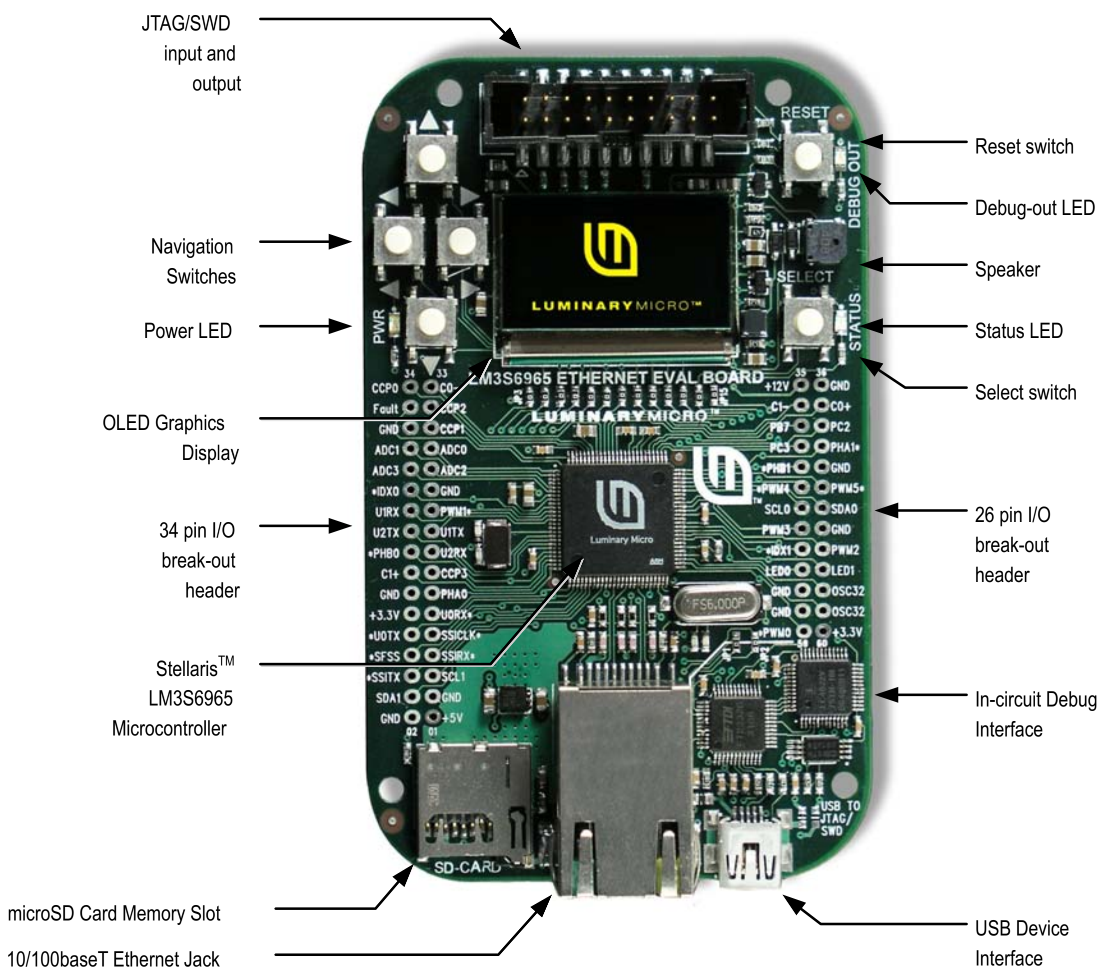
Stellaris® LM3S6965 Evaluation Board

The Stellaris® LM3S6965 Evaluation Board is a compact and versatile evaluation platform for the Stellaris LM3S6965 ARM® Cortex™-M3-based microcontroller. The evaluation kit uses the LM3S6965 microcontroller's fully integrated 10/100 Ethernet controller to demonstrate an embedded web server.

You can use the board either as an evaluation platform or as a low-cost in-circuit debug interface (ICDI). In debug interface mode, the on-board microcontroller is bypassed, allowing programming or debugging of an external target. The kit is also compatible with high-performance external JTAG debuggers.

This evaluation kit enables quick evaluation, prototype development, and creation of application-specific designs for Ethernet networks. The kit also includes extensive source-code examples, allowing you to start building C code applications quickly.

Figure 1-1. Stellaris LM3S6965 Evaluation Board Layout



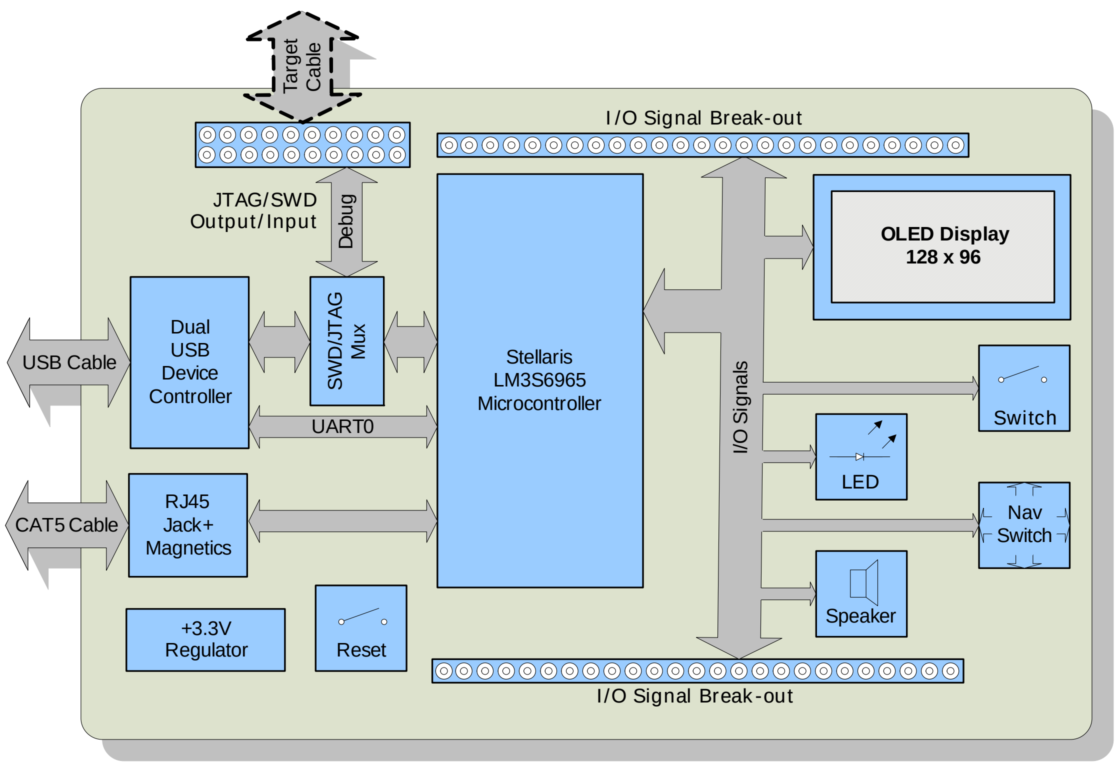
Features

The Stellaris LM3S6965 Evaluation Board includes the following features:

- Stellaris LM3S6965 microcontroller with fully-integrated 10/100 embedded Ethernet controller
- Simple setup; USB cable provides serial communication, debugging, and power
- OLED graphics display with 128 x 96 pixel resolution
- User LED, navigation switches, and select pushbuttons
- Magnetic speaker
- LM3S6965 I/O available on labeled break-out pads
- Standard ARM® 20-pin JTAG debug connector with input and output modes
- USB interface for debugging and power supply
- MicroSD card slot

Block Diagram

Figure 1-2. LM3S6965 Evaluation Board Block Diagram



Evaluation Kit Contents

The evaluation kit contains everything needed to develop and run applications for Stellaris microcontrollers including:

- LM3S6965 Evaluation Board (EVB)
- USB cable
- 20-pin JTAG/SWD target cable
- CD containing:
  - A supported version of one of the following (including a toolchain-specific Quickstart guide):
    - Keil™ RealView® Microcontroller Development Kit (MDK-ARM)
    - IAR Embedded Workbench
    - Code Sourcery GCC development tools
    - Code Red Technologies development tools
    - Texas Instruments' Code Composer Studio™ IDE
  - Complete documentation
  - Quickstart application source code
  - Stellaris® Firmware Development Package with example source code

Evaluation Board Specifications

- Board supply voltage: 4.37–5.25 Vdc from USB connector
- Board supply current: 250 mA typ (fully active, CPU at 50 MHz)
- Break-out power output: 3.3 Vdc (60 mA max), 15 Vdc (15 mA max)
- Dimensions: 4.0" x 2.45" x 0.7" (LxWxH)
- RoHS status: Compliant

Features of the LM3S6965 Microcontroller

- 32-bit RISC performance using ARM® Cortex™-M3 v7M architecture
  - 50-MHz operation
  - Hardware-division and single-cycle-multiplication
  - Integrated Nested Vectored Interrupt Controller (NVIC)
  - 42 interrupt channels with eight priority levels
- 256 KB single-cycle Flash
- 64 KB single-cycle SRAM
- Four general-purpose 32-bit timers
- Integrated Ethernet MAC and PHY
- Three fully programmable 16C550-type UARTs
- Four 10-bit channels (inputs) when used as single-ended inputs

- Two independent integrated analog comparators
- Two I^{2}C modules
- Three PWM generator blocks
  - One 16-bit counter
  - Two comparators
  - Produces two independent PWM signals
  - One dead-band generator
- Two QEI modules with position integrator for tracking encoder position
- 0 to 42 GPIOs, depending on user configuration
- On-chip low drop-out (LDO) voltage regulator

CHAPTER 2

Hardware Description

In addition to a microcontroller, the Stellaris LM3S6965 evaluation board includes a range of useful peripherals and an integrated ICDI. This chapter describes how these peripherals operate and interface to the MCU.

LM3S6965 Microcontroller

Device Overview

The heart of the EVB is a Stellaris LM3S6965 ARM Cortex-M3-based microcontroller. The LM3S6965 offers 256 KB Flash memory, 50-MHz operation, an Ethernet controller, and a wide range of peripherals. Refer to the LM3S6965 data sheet (order number DS-LM3S6965) for complete device details.

The LM3S6965 microcontroller is factory programmed with a quickstart demo program. The quickstart program resides in the LM3S6965 on-chip Flash memory and runs each time power is applied, unless the quickstart has been replaced with a user program.

Ethernet

A key feature of the LM3S6965 microcontroller is its fully integrated Ethernet controller. Only a RJ45 jack with integrated magnetics and a few passive components are needed to complete the 10/100baseT interface. The RJ45 jack incorporates LEDs that indicate traffic and link status. These are automatically managed by on-chip microcontroller hardware. Alternatively, the LEDs can be software controlled by configuring those pins as general-purpose outputs.

The LM3S6965 supports automatic MDI/MDI-X so the EVB can connect directly to a network or to another Ethernet device without requiring a cross-over cable.

Clocking

The LM3S6965 microcontroller has four on-chip oscillators, three are implemented on the EVB. A 8.0-MHz crystal completes the LM3S6965's main internal clock circuit. An internal PLL, configured in software, multiples this clock to 50-MHz for core and peripheral timing.

A small, 25-MHz crystal is used by the LM3S6965 microcontroller for Ethernet physical layer timing and is independent of the main oscillator.

Reset

The LM3S6965 microcontroller shares its external reset input with the OLED display. In the EVB, reset sources are gated through the CPLD, though in a typical application a simple wired-OR arrangement is sufficient.

Reset is asserted (active low) under any one of three conditions:

- Power-on reset
- Reset push switch SW1 held down
- Internal debug mode—By the USB device controller (U4 FT2232) when instructed by debugger

Power Supplies

The LM3S6965 is powered from a +3.3-V supply. A low drop-out (LDO) regulator regulates +5-V power from the USB cable to +3.3-V. +3.3-V power is available for powering external circuits.

A +15-V rail is available when the OLED display is active. The speaker and OLED display boost-converter operate directly from the +5-V rail.

Debugging

Stellaris microcontrollers support programming and debugging using either JTAG or SWD. JTAG uses the signals `TCK`, `TMS`, `TDI`, and `TDO`. SWD requires fewer signals (`SWCLK`, `SWDIO`, and, optionally, `SWO`, for trace). The debugger determines which debug protocol is used.

Debugging Modes

The LM3S6965 evaluation board supports a range of hardware debugging configurations. Table 2-1 summarizes these configurations.

Table 2-1. Stellaris LM3S6965 Evaluation Board Hardware Debugging Configurations

Mode	Debug Function	Use	Selected by
1	Internal ICDI	Debug on-board LM3S6965 microcontroller over USB interface.	Default mode
2	ICDI out to JTAG/SWD header	The EVB is used as a USB to SWD/JTAG interface to an external target.	Connecting to an external target and starting debug software. The red Debug Out LED will be ON.
3	In from JTAG/SWD header	For users who prefer an external debug interface (ULINK, JLINK, etc.) with the EVB.	Connecting an external debugger to the JTAG/SWD header.

Modes 2 and 3 automatically detect the presence of an external debug cable. When the debugger software is connected to the EVB's USB controller, the EVB automatically selects Mode 2 and illuminates the red Debug Out LED.

Debug In Considerations

Debug Mode 3 supports evaluation board debugging using an external debug interface. Mode 3 is automatically selected when a device such as a Segger J-Link or Keil ULINK is connected.

Boards marked Revision D or later automatically configure pin 1 to be a 3.3-V reference, if an external debugger is connected. To determine the revision of your board, locate the product number on the bottom of the board; for example, EK-LM3S6965-D. The last character of the product number identifies the board revision.

A configuration or board-level change may be necessary when using an external debug interface with revisions A through C of this evaluation board. Because the evaluation board supports both debug out and debug in modes, pin 1 of the 20-pin JTAG/SWD header is, by default, not connected to +3.3 V. Consequently, devices requiring a voltage on pin 1 to power their line buffers may not work.

Two solutions exist. Some debugger interfaces (such as ULINK) have an internal power jumper that, in this case, should be set to internal +3.3-V power. Refer to debugger interface

documentation for full details. However, if your debugger interface does not have a selectable power source, it may be necessary to install a 0-Ω resistor on the evaluation board to route power to pin 1. Refer to the schematics and board drawing in the appendix of this manual for the location of this resistor.

USB Device Controller Functions

Device Overview

An FT2232 device from Future Technology Devices International Ltd manages USB-to-serial conversion. The FT2232 is factory configured to implement a JTAG/SWD port (synchronous serial) on channel A and a Virtual COM Port (VCP) on channel B. This feature allows two simultaneous communications links between the host computer and the target device using a single USB cable. Separate Windows drivers for each function are provided on the Documentation and Software CD.

A small serial EEPROM holds the FT2232 configuration data. The EEPROM is not accessible by the LM3S6965 microcontroller.

For full details on FT2232 operation, go to www.ftdichip.com.

USB to JTAG/SWD

The FT2232 USB device performs JTAG/SWD serial operations under the control of the debugger. A CPLD (U2) multiplexes SWD and JTAG functions and, when working in SWD mode, provides direction control for the bidirectional data line.

Virtual COM Port

The Virtual COM Port (VCP) allows Windows applications (such as HyperTerminal) to communicate with `UART0` on the LM3S6965 over USB. Once the FT2232 VCP driver is installed, Windows assigns a COM port number to the VCP channel.

Serial Wire Out

The evaluation board supports the Cortex-M3 serial-wire output (SWO) trace capabilities. Under debugger control, the CPLD can route the SWO datastream to the virtual communication port (VCP) transmit channel. The debugger can then decode and interpret the trace information received from the VCP. The normal VCP connection to `UART0` is interrupted when using SWO. Not all debuggers support SWO. Refer to the Stellaris LM3S6965 data sheet for additional information on the trace port interface unit (TPIU).

Organic LED Display

The EVB features an organic LED (OLED) graphics display with 128 x 96 pixel resolution. OLED is a new technology that offers many advantages over LCD display technology.

Features

- RiT P14201 series display
- 128 columns by 96 rows
- High-contrast (typ. 500:1)
- Excellent brightness (120 cd/m^2)
- Fast 10 us response

Control Interface

The OLED display has a built-in controller IC with synchronous serial and parallel interfaces. Synchronous serial (SSI) is used on the EVB as it requires fewer microcontroller pins. Data cannot be read from the OLED controller; only one data line is necessary. Note that the SSI port is shared with the microSD card slot. The Stellaris® Firmware Development Package (included on the Documentation and Software CD) contains complete drivers with source-code for the OLED display.

Power Supply

A +15-V supply is needed to bias the OLED display. A FAN5331 device from Fairchild combines with a few external components to complete a boost converter. When the OLED display is operating, a small amount of power can be drawn from the +15-V rail to power other devices.

Design Guidelines

The OLED display has a lifetime of about 13,000 hours. It is also prone to degradation due to burn-in, similar to CRT and plasma displays. The quickstart application includes both a screen saver and a power-down mode to extend display life. These factors should be considered when developing EVB applications that use the OLED display.

When using the EVB as an in-circuit debug interface (ICDI), the OLED display is held in reset to reduce power consumption and eliminate display wear-out.

Further Reference

For additional information on the RiT OLED display, visit www.ritekdisplay.com.

Other Peripherals

Speaker

A small, magnetic audio transducer connects through a MOSFET to `PD1/PWM1`, allowing a range of options for generating simple and complex tones. Use of the +5-V rail reduces switching noise on the +3.3-V rail.

MicroSD Card Slot

Removable Flash cards are an ideal media for storing data such as web page content. The source code on the CD includes example code for reading data from standard FAT formatted SD cards. All data and control transactions use the SD card’s SPI mode. Note that the SD card specification does not require that a card supports the SPI mode, but most cards do so in practice. Cards from several vendors have been used with the EVB.

MicroSD cards are very small and require careful handling. the SD card slot on the EVB is a push-push type (push to insert; push again to eject).

Note: To avoid damage, *remove power before inserting or removing cards*.The EVB does not implement SD card power control.

Push Switches

The EVB has five general-purpose input switches. Four are arranged in a navigation-style configuration. The fifth functions as a Select switch.

User LED

A user LED (LED3) is provided for general use. The LED is connected to `PC5/CCP1`, allowing the option of either GPIO or PWM control (brightness control). Refer to the Quickstart Application source code for an example of PWM control.

Bypassing Peripherals

Excluding Ethernet, the EVB's on-board peripheral circuits require 16 GPIO lines. Two additional GPIO lines are assigned to Ethernet LEDs. This leaves 20 GPIO lines and 4 ADC channels immediately available for connection to external circuits. If an application requires more GPIO lines, the on-board hardware can be disconnected. The EVB is populated with 16 jumper links, which can be cut with a knife to isolate on-board hardware. The process can be reversed by installing 0603- 0-ohm chip resistors.

Important*:* The quickstart application will not run if one or more jumpers are removed.

Table 2-2. Isolating On-Board Hardware

MCU Pin	EVB Function	To Isolate, Remove...
Pin 26 `PA0/U0RX`	Virtual COM port receive	JP1
Pin 27 `PA1/U0TX`	Virtual COM port transmit	JP2
Pin 10 `PD0/IDX0`	SD card chip select	JP3
Pin 11 `PD1/PWM1`	Sound	JP4
Pin 30 `PA4/SSI0RX`	SD card data out	JP5
Pin 31 `PA5/SSI0TX`	SD card and OLED display data in	JP6
Pin 28 `PA2/SSI0CLK`	SD card and OLED display clock	JP7
Pin 22 `PC7/PHB0`	OLED display data/control select	JP8
Pin 29 `PA3/SSI0FSS`	OLED display chip select	JP9
Pin 73 `PE1/PWM5`	Down switch	JP10
Pin 74 `PE2/PHB1`	Left switch	JP11
Pin 72 `PE0/PWM4`	Up switch	JP12
Pin 75 `PE3/PHA1`	Right switch	JP13
Pin 61 `PF1/IDX1`	Select switch	JP14
Pin 47 `PF0/PWM0`	User LED	JP15
Pin 23 `PC6/CCP3`	Enable +15 V	JP16

Interfacing to the EVB

An array of accessible I/O signals makes it easy to interface the EVB to external circuits. All LM3S6965 I/O lines (except those with both JTAG and SWD functions) are brought out to 0.1" pitch pads. For quick reference, silk-screened labels on the PCB show primary pin functions.

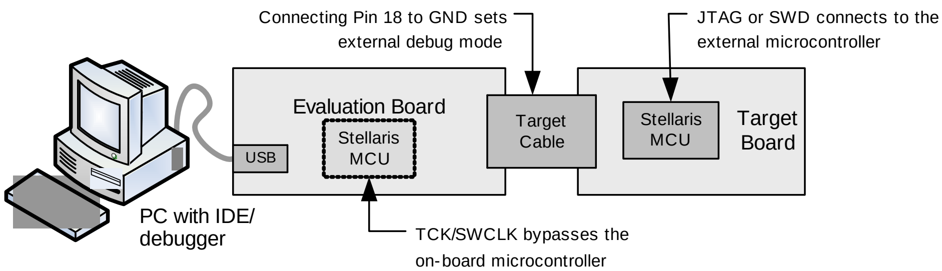
Table B-1 on page 25 has a complete list of I/O signals as well as recommended connectors.

Most LM3S6965 I/O signals are +5-V tolerant. Refer to the LM3S6965 data sheet for detailed electrical specifications.

Using the In-Circuit Debugger Interface

The Stellaris LM3S6965 Evaluation Kit can operate as an In-Circuit Debugger Interface (ICDI). ICDI acts as a USB to the JTAG/SWD adaptor, allowing debugging of any external target board that uses a Stellaris microcontroller. See “Debugging Modes” on page 12 for a description of how to enter Debug Out mode.

Figure 2-1. ICD Interface Mode



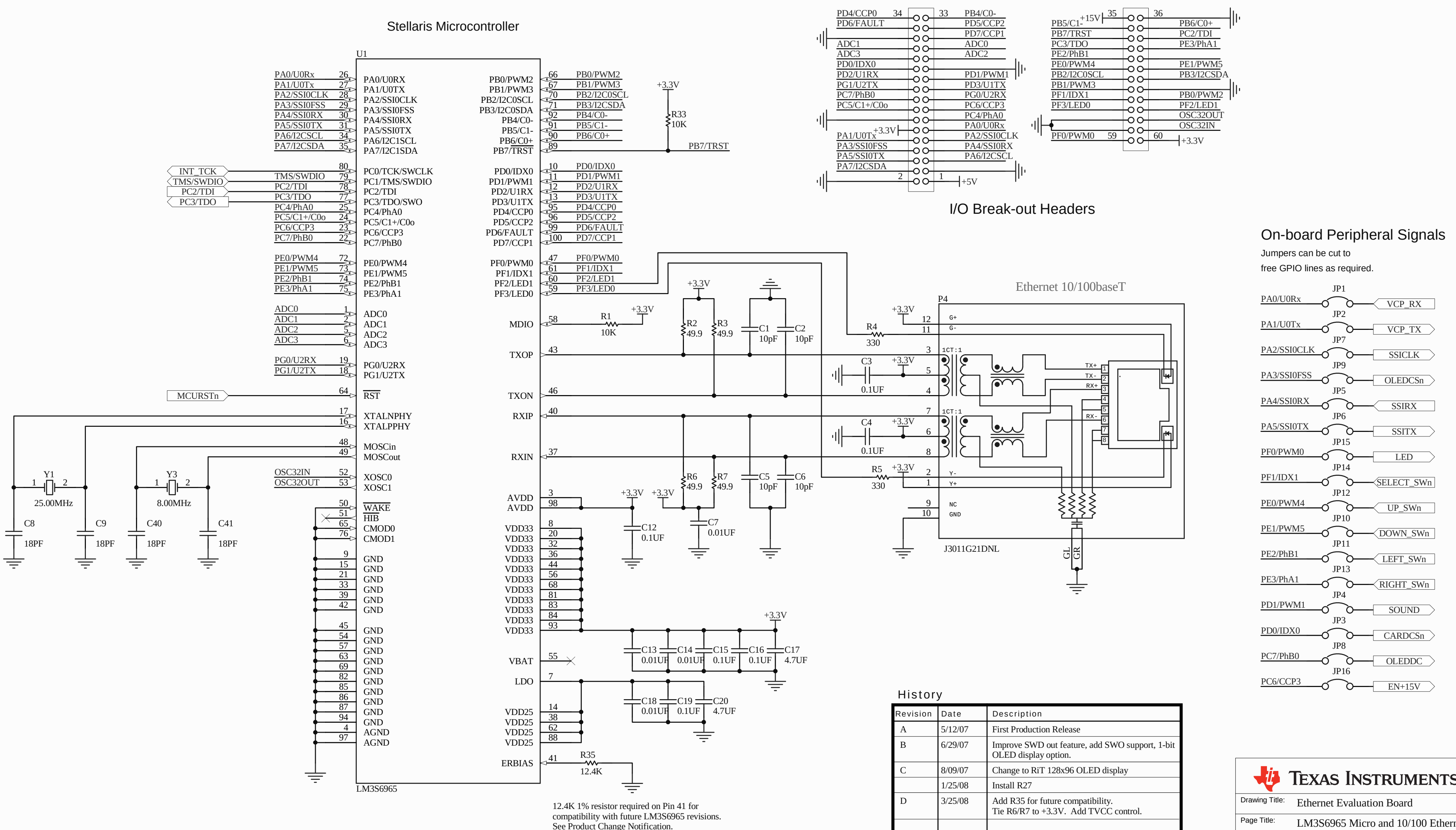
The debug interface operates in either Serial-Wire Debug (SWD) or full JTAG mode, depending on the configuration in the debugger IDE.

The IDE/debugger does not distinguish between the on-EVB Stellaris microcontroller and an external Stellaris microcontroller. The only requirement is that the correct Stellaris device is selected in the project configuration.

A P P E N D I X A

Schematics

This section contains the schematics for the LM3S6965 evaluation board:



History

Revision	Date	Description
A	5/12/07	First Production Release
B	6/29/07	Improve SWD out feature, add SWO support, 1-bit OLED display option.
C	8/09/07	Change to RiT 128x96 OLED display
	1/25/08	Install R27
D	3/25/08	Add R35 for future compatibility. Tie R6/R7 to +3.3V. Add TVCC control.

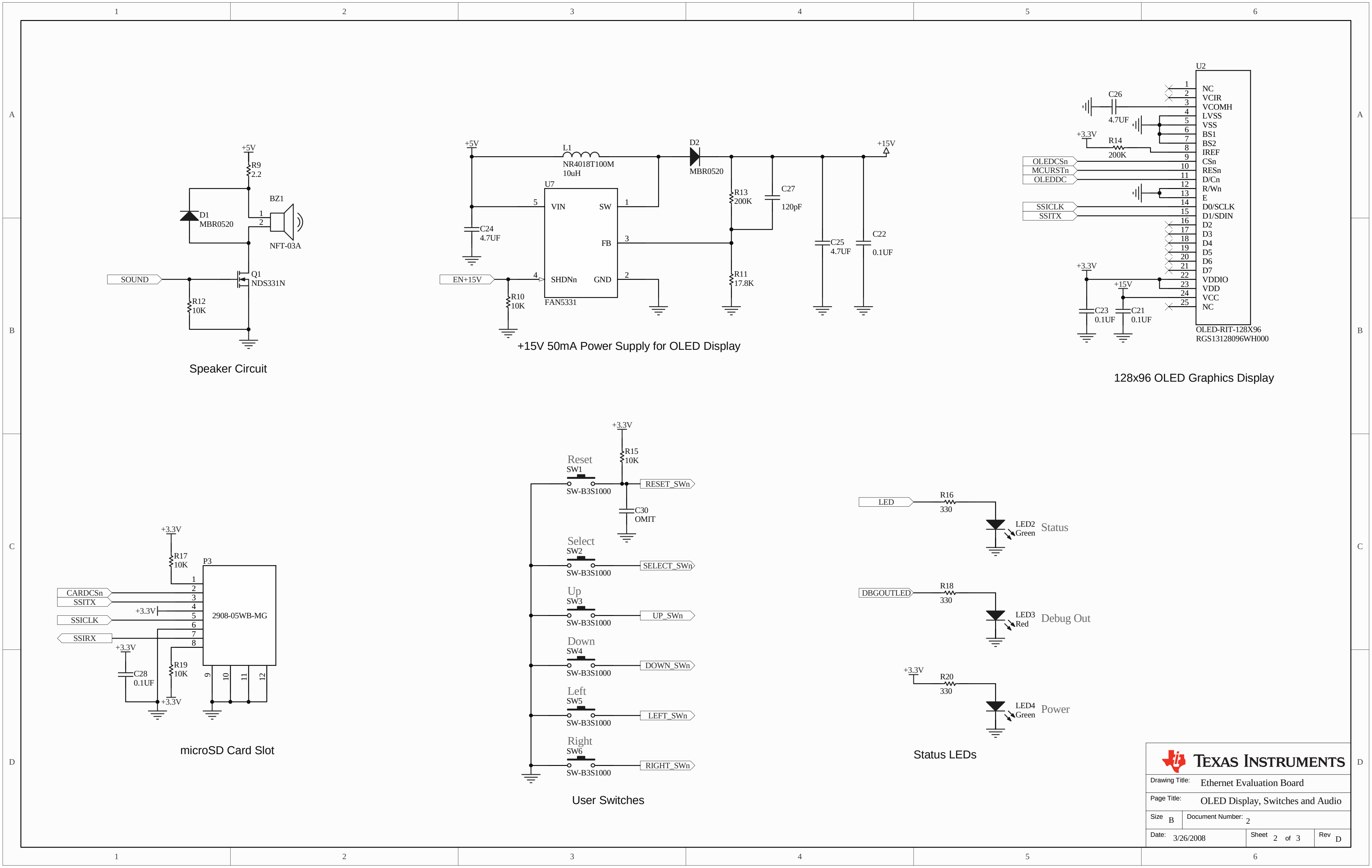
TEXAS INSTRUMENTS

Drawing Title: Ethernet Evaluation Board

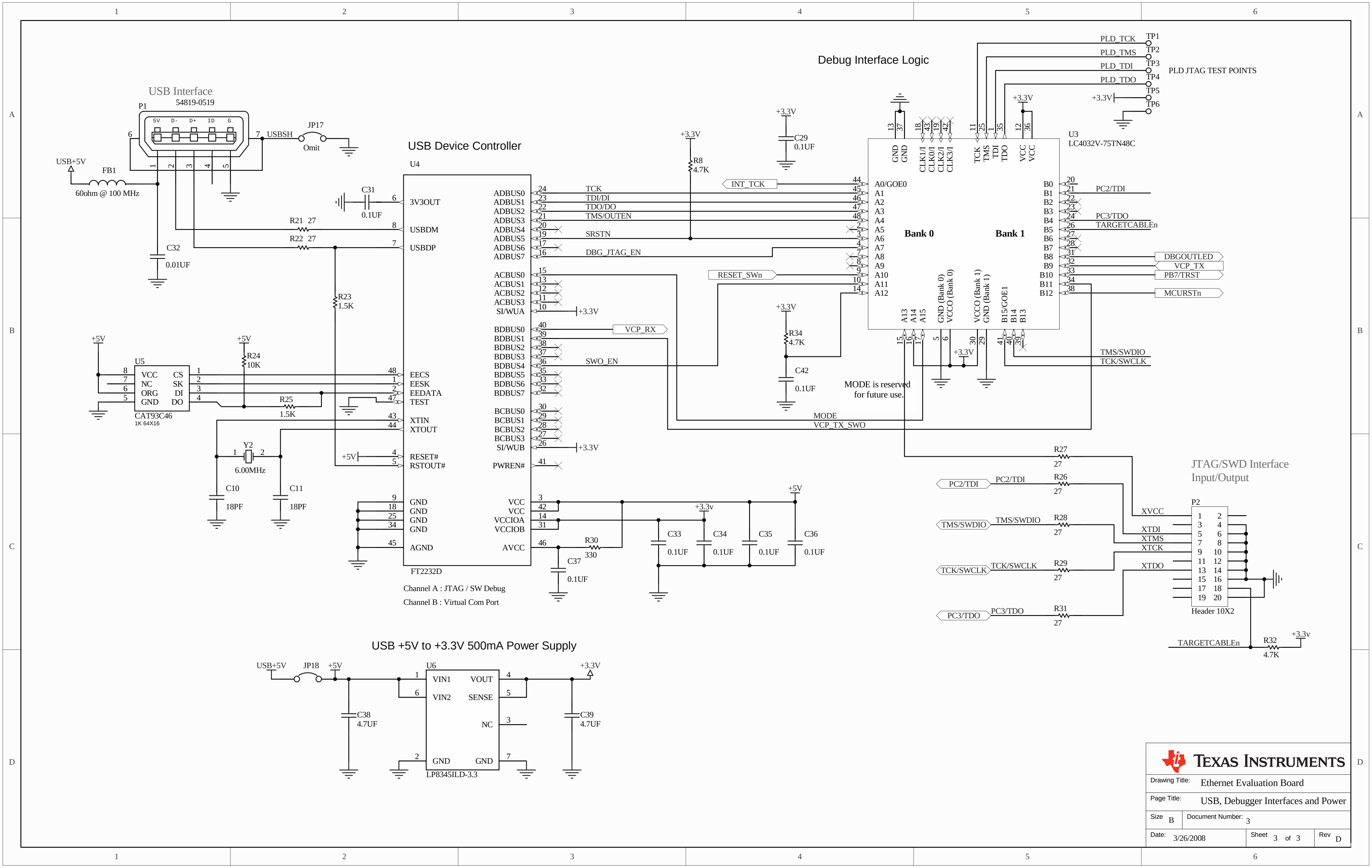
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Size B | Document Number: 1

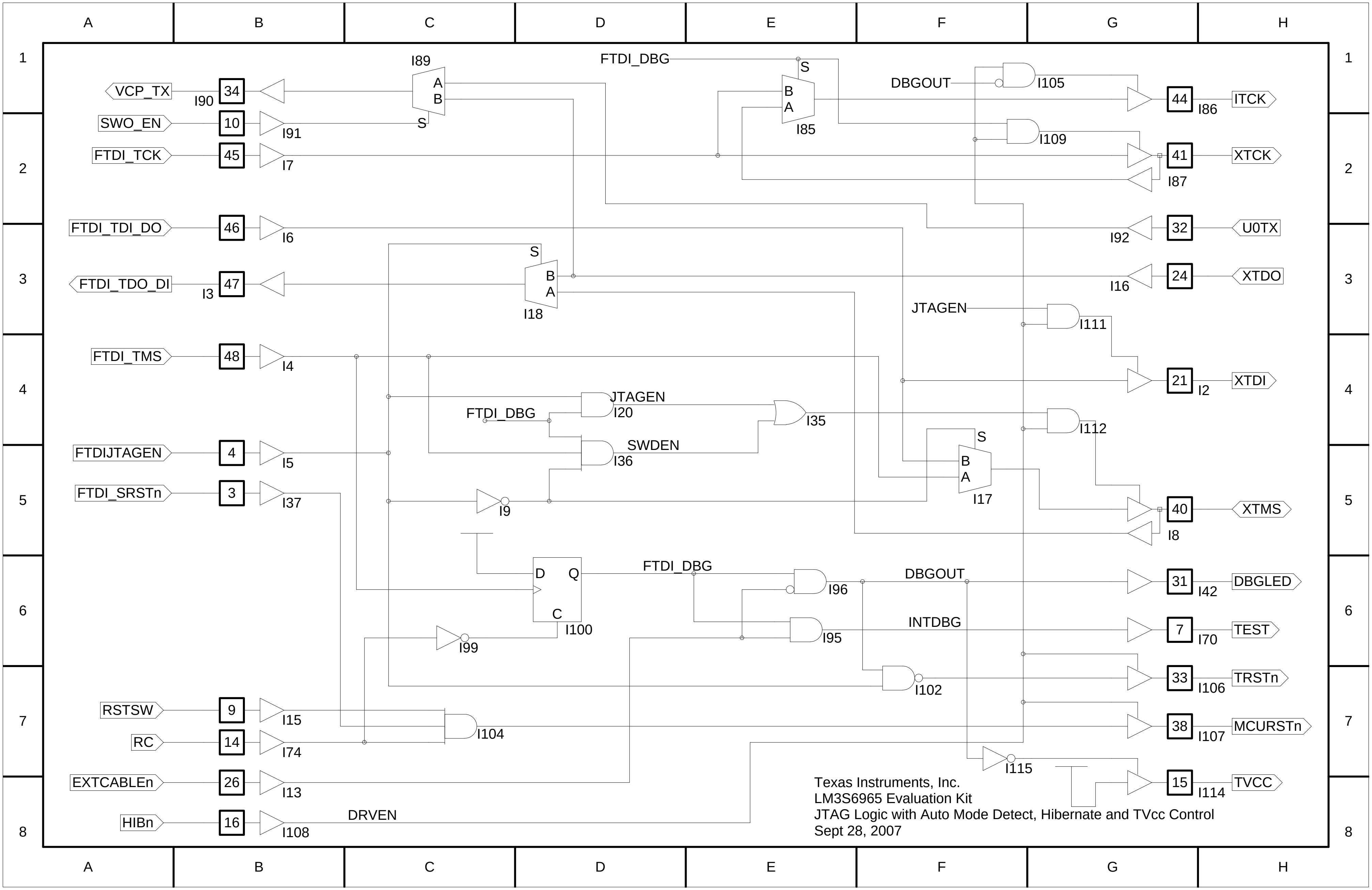
Date: 3/26/2008 | Sheet 1 of 3 | Rev D



Speaker Circuit
+5V
R9 2.2
D1 MBR0520
BZ1 NFT-03A
SOUND
Q1 NDS331N
R12 10K
+15V 50mA Power Supply for OLED Display
+5V
L1 NR4018T100M 10uH
D2 MBR0520
+15V
U7 FAN5331
VIN SW FB SHDNn GND
C24 4.7UF
EN+15V
R10 10K
R13 200K
C27 120pF
R11 17.8K
C25 4.7UF
C22 0.1UF
128x96 OLED Graphics Display
U2 OLED-RIT-128X96 RGS13128096WH000
NC VCIR VCOMH LVSS VSS BS1 BS2 IREF CSn RESn D/Cn R/Wn E D0/SCLK D1/SDIN D2 D3 D4 D5 D6 D7 VDDIO VDD VCC NC
C26 4.7UF
+3.3V
R14 200K
OLEDCSn
MCURSTn
OLEDDC
SSICLK
SSITX
C23 0.1UF
C21 0.1UF
+15V
microSD Card Slot
P3 2908-05WB-MG
R17 10K
CARDCSn
SSITX
SSICLK
SSIRX
C28 0.1UF
R19 10K
User Switches
+3.3V
R15 10K
C30 OMIT
Reset SW1 SW-B3S1000 RESET_SWn
Select SW2 SW-B3S1000 SELECT_SWn
Up SW3 SW-B3S1000 UP_SWn
Down SW4 SW-B3S1000 DOWN_SWn
Left SW5 SW-B3S1000 LEFT_SWn
Right SW6 SW-B3S1000 RIGHT_SWn
Status LEDs
LED R16 330 LED2 Green Status
DBGOUTLED R18 330 LED3 Red Debug Out
+3.3V R20 330 LED4 Green Power
TEXAS INSTRUMENTS
Drawing Title: Ethernet Evaluation Board
Page Title: OLED Display, Switches and Audio
Size B Document Number: 2
Date: 3/26/2008 Sheet 2 of 3 Rev D



Debug Interface Logic
USB Interface
54819-0519
P1
USBSH
JP17
Omit
USB+5V
FB1
60ohm @ 100 MHz
C32
0.01UF
R21 27
R22 27
R23
1.5K
C31
0.1UF
USB Device Controller
U4
3V3OUT
USBDM
USBDP
EECS
EESK
EEDATA
TEST
XTIN
XTOUT
RESET#
RSTOUT#
GND
AGND
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
SI/WUA
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
SI/WUB
PWREN#
VCC
VCCIOA
VCCIOB
AVCC
FT2232D
Channel A : JTAG / SW Debug
Channel B : Virtual Com Port
TCK
TDI/DI
TDO/DO
TMS/OUTEN
SRSTN
DBG_JTAG_EN
VCP_RX
SWO_EN
MODE
VCP_TX_SWO
U5
VCC
NC
ORG
GND
CS
SK
DI
DO
CAT93C46
1K 64X16
R24
10K
R25
1.5K
Y2
6.00MHz
C10
18PF
C11
18PF
R30
330
C37
0.1UF
C33
0.1UF
C34
0.1UF
C35
0.1UF
C36
0.1UF
R8
4.7K
C29
0.1UF
INT_TCK
RESET_SWn
R34
4.7K
C42
0.1UF
MODE is reserved for future use.
U3
LC4032V-75TN48C
Bank 0
Bank 1
A0/GOE0
B15/GOE1
VCCO (Bank 0)
GND (Bank 0)
VCCO (Bank 1)
GND (Bank 1)
PC2/TDI
PC3/TDO
TARGETCABLEn
DBGOUTLED
VCP_TX
PB7/TRST
MCURSTn
TMS/SWDIO
TCK/SWCLK
PLD_TCK
PLD_TMS
PLD_TDI
PLD_TDO
TP1
TP2
TP3
TP4
TP5
TP6
PLD JTAG TEST POINTS
JTAG/SWD Interface Input/Output
P2
XVCC
XTDI
XTMS
XTCK
XTDO
Header 10X2
R26
R27
R28
R29
R31
27
R32
4.7K
USB +5V to +3.3V 500mA Power Supply
JP18
U6
VIN1
VIN2
VOUT
SENSE
NC
GND
LP8345ILD-3.3
C38
4.7UF
C39
4.7UF
+5V
+3.3V
Texas Instruments
Drawing Title: Ethernet Evaluation Board
Page Title: USB, Debugger Interfaces and Power
Size B
Document Number: 3
Date: 3/26/2008
Sheet 3 of 3
Rev D



VCP_TX
SWO_EN
FTDI_TCK
FTDI_TDI_DO
FTDI_TDO_DI
FTDI_TMS
FTDIJTAGEN
FTDI_SRSTn
RSTSW
RC
EXTCABLEn
HIBn
FTDI_DBG
DBGOUT
JTAGEN
SWDEN
INTDBG
DRVEN
ITCK
XTCK
U0TX
XTDO
XTDI
XTMS
DBGLED
TEST
TRSTn
MCURSTn
TVCC
I89
I85
I105
I109
I86
I87
I90
I91
I7
I6
I3
I18
I92
I16
I111
I4
I2
I20
I35
I36
I112
I5
I17
I37
I9
I8
I100
I96
I42
I95
I70
I99
I102
I106
I15
I104
I107
I74
I115
I13
I114
I108
Texas Instruments, Inc.
LM3S6965 Evaluation Kit
JTAG Logic with Auto Mode Detect, Hibernate and TVcc Control
Sept 28, 2007

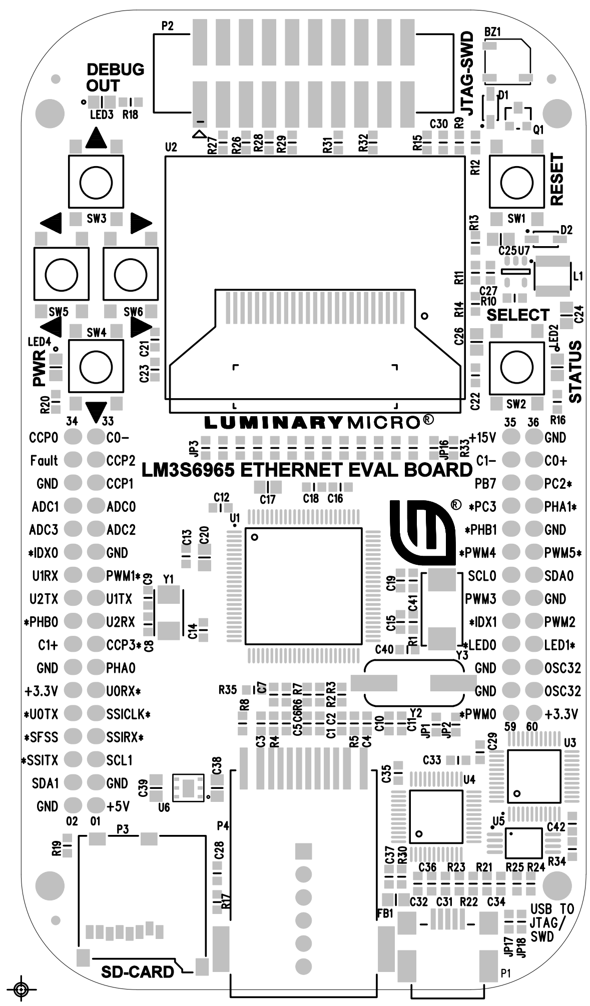
Connection Details

This appendix contains the following sections:

- Component Locations
- Evaluation Board Dimensions
- I/O Breakout Pads
- ARM Target Pinout

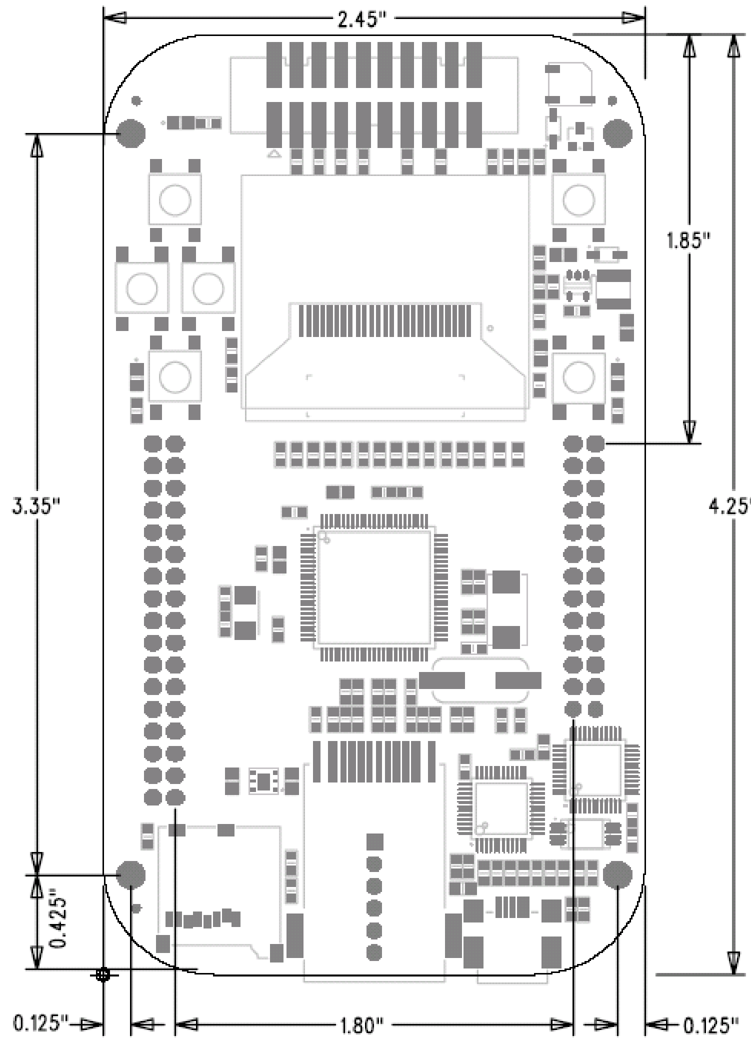
Component Locations

Figure B-1. Component Locations



Evaluation Board Dimensions

Figure B-2. Evaluation Board Dimensions



I/O Breakout Pads

The LM3S6965 EVB has 44 I/O pads, 14 power pads, and 2 crystal connections, for a total of 60 pads. Connection can be made by soldering wires directly to these pads, or by using 0.1” pitch headers and sockets.

Note: In Table B-2, an asterisk (*) by a signal name (also on the EVB PCB) indicates the signal is normally used for on-board functions. Normally, you should cut the associated jumper (JP1-15) before using an assigned signal for external interfacing.

Table B-1. I/O Breakout Pads

Description	Pad No.	Pad No.	Description	Description	Pad No.	Pad No.	Description
PD4/CCP0	34	33	PB4/C0-	+12 V	35	36	GND
PD6/FAULT	32	31	PD5/CCP2	PB5/C1-	37	38	PB6/C0+
GND	30	29	PD7/CCP1	PB7/$\overline{TRST}$	39	40	PC2/TDI*
ADC1	28	27	ADC0	PC3/TDO*	41	42	PE3/PHA1*
ADC3	26	25	ADC2	PE2/PHB1*	43	44	GND
IDX0*	24	23	GND	PE0/PWM4*	45	46	PE1/PWM5*
PD2/U1RX	22	21	PD1/PWM1*	PB2/SCL0	47	48	PB3/SDA0
PG1/U2TX	20	19	PD3/U1TTX	PB1/PWM3	49	50	GND
PC7/PHB0*	18	17	PG0/U2RX	PF1/IDX1*	51	52	PB0/PWM2
PC5/C1+	16	15	PC6/CCP3*	PF3/LED0	53	54	PF2/LED1
GND	14	13	PC4/PHA0	GND	55	56	OSC32
+3.3 V	12	11	PA0/U0RX*	GND	57	58	OSC32
PA1/U0TX*	10	9	PA2/SSICLK*	PF0/PWM0*	59	60	+3.3 V
PA3/SFSS*	8	7	PA4/SSIRX*				
PA5/SSITX*	6	5	PA6/SCL1				
PA7/SDA1	4	3	GND				
GND	2	1	+5 V				

Recommended Connectors

Connection can be made by soldering wires directly to pads or using 0.1” pitch headers and sockets.

Table B-2. Recommended Connectors

Pins 1-34 (2 x 17 way)	PCB Socket	Sullins PPPC172LFBN-RC	Digikey S7120-ND
	Cable Socket	3M 89134-0101	Digikey MKC34A-ND
	Pin Header	Sullins PEC17DAAN	Digikey S2012E-17-ND
Pins 35-06 (2 x 13 way)	PCB Socket	Sullins PPPC132LFBN-RC	Digikey S7116-ND
	Cable Socket	3M 89126-0101	Digikey MKC26A-ND
	Pin Header	Sullins PEC13DAAN	Digikey S2012-13-ND

ARM Target Pinout

In ICDI input and output mode, the Stellaris LM3S6965 Evaluation Kit supports ARM's standard 20-pin JTAG/SWD configuration. The same pin configuration can be used for debugging over Serial Wire Debug (SWD) and JTAG interfaces. The debugger software, running on the PC, determines which interface protocol is used.

The Stellaris target board should have a 2x10 0.1" pin header with signals as indicated in Table B-3. This applies to both an external Stellaris MCU target (Debug output mode) and to external JTAG/SWD debuggers (Debug input mode).

Table B-3. 20-Pin JTAG/SWD Configuration

Function	Pin	Pin	Function
VCC	1	2	nc
nc	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
NC	11	12	GND
TDO	13	14	GND
nc	15	16	GND
nc	17	18	GND
nc	19	20	GND

ICDI does not control $\overline{\text{RST}}$ (device reset) or $\overline{\text{TRST}}$ (test reset) signals. Both reset functions are implemented as commands over JTAG/SWD, so these signals are not necessary.

It is recommended that connections be made to all GND pins; however, both targets and external debug interfaces must connect pin 18 and at least one other GND pin to GND.

References

In addition to this document, the following references are included on the Stellaris® LM3S6965 Evaluation Kit documentation CD-ROM and are also available for download at www.ti.com/stellaris:

- *Stellaris LM3S6965 Evaluation Kit Quickstart Guide* for appropriate tool kit (see "Evaluation Kit Contents," on page 10)
- *Stellaris LM3S6965 Read Me First* for the CAN Evaluation Kit
- StellarisWare® Driver Library, Order number SW-DRL
- *StellarisWare® Driver Library User's Manual*, publication number SW-DRL-UG
- *Stellaris LM3S6965 Data Sheet*, publication DS-LM3S6965

Additional references include:

- *Future Technology Devices Incorporated FT2232C Datasheet*
- Information on development tool being used:
  - RealView MDK web site, www.keil.com/arm/rvmdkkit.asp
  - IAR Embedded Workbench web site, www.iar.com
  - Code Sourcery GCC development tools web site, www.codesourcery.com/gnu_toolchains/arm
  - Code Red Technologies development tools web site, www.code-red-tech.com
  - Texas Instruments' Code Composer Studio™ IDE web site, www.ti.com/ccs

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